ABHIGYAN YERRA

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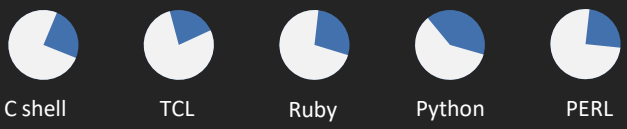
SUMMARY

A Senior Design Engineer with over 6 years experience in ASIC designing and implementation, working with Qualcomm for the development of Semiconductors. Offers expertise in all aspects of digital design, Verification, Failure Analysis and tool runs for implementation.

AREAS OF EXPERTISE

- In-depth knowledge of **PIB bus and AMBA bus protocols**.
- Hands-on experience in Digital Design, Design Scripting, Design Implementation and Design Verification.
- Hands-on experience in RTL Design Linting, UPF file Generation, Conformal low power analysis, power-aware Synthesis, Formal Verification, Static Timing Analysis, RTL power Analysis and CDC (Clock Domain Crossing).
- Worked on **Spyglass and Cadence tools.**
- Expertise in **Perl, Python, Ruby and C shell Scripting.**
- Familiar with **TCL scripting.**

SCRIPTING LANGUAGES



CAREER TIMELINE

Jan 2017 – Present
Qualcomm, India
Senior Design Engineer – Front End Design/Scripting

Apr 2016 – Dec 2016
SoCtronics Technologies, India
Engineer II - Front End Design/ Verification/Scripting

Jul 2013 – Mar 2016
SoCtronics Technologies, India
Engineer I - Front End Design/ Verification/Scripting

PROFESSIONAL EXPERIENCE

Jan 2017 – Present

Qualcomm, India | Senior Design Engineer - Front End Design/Scripting

Devise Front End Design and Scripting in the capacity of a Senior Design Engineer for multiple projects, responsible for the complete designing and implementation methodology of the Semiconductor including, static timing/crosstalk analysis, primetime and analog - digital port mapping for communication between Analog and digital, as per analog requirements. The design went through various tool runs throughout the various projects, measuring to linting checks and waivers generation, unified power format file generation using power intent engine, conformal low power analysis(CLP), constraints creation for synthesis, power-aware synthesis, formal verification, static timing analysis, clock domain crossing, and engineering change orders(ECO).

Design and Implementation of register digital tops:

- Design and implement Register Digital top modules on multiple projects by updating the Analog-Digital Mapping XML on the requirements.
- Update the digital register mapping XML, run XML through scripts, solve prebuild errors, generate the register module, generate the RTL on top of the register module, ensure implementation of DFT coding.
- When required, update the script to get desired functionality on register file, implementation of which includes Linting, UPF, CLP, synthesis, FV, STA, CDC and ECO.
- Projects: Axion, Streamer, Beamer, Beamer2.0, Magnus, Magnus2.0, Caster, Electron.

TECHNICAL SKILLS

EDA Tools:

- SpyGlass Linting
- UPF file creation
- Conformal Low Power Analysis
- Synopsis Design compiler and Cadence Genus for power-aware synthesis
- Cadence Conformal
- Spyglass and CDC
- Synopsys Primetime
- Cadence Conformal ECO
- Cadence NCSIM
- RTL compiler
- RTL power Analysis.

Implementation and Testing:

- Linting checks and waivers generation
- Unified power format file generation using Power Intent Engine
- Conformal Low power Analysis(CLP)
- Constraints creation for Synthesis
- power Aware Synthesis
- Formal Verification
- Static Timing Analysis
- Clock Domain Crossing
- Engineering Change Orders(ECO) and CDC (Clock Domain Crossing).

HD/HV Languages:

- Verilog
- System Verilog

Implementation of Engineering Change Order

- Implement 2 level ECO and Digital Subsystem module, generate patch code and verify using conformal LEC tool in Tachyon project.
- Updated and created generic makefile file flow for easy implementation of ECO RTL to PD netlist and reduced the human effort to setup ECO files. Also, used this generic ECO setup in multiple projects.
- Projects: Tachyon, Cheops, Disruptor, Disruptor 2.0, RIOT, RIOT2.0, Phaser, phaser 2.0, Beamer, Beamer 2.0, Magnus, Magnus 2.0.

Implementation of Digital Modules

- Implementation of complex modules, which includes IDT (Integrated Design for test) UPF file generation, IDT (Integrated Design for test) block file generation, CLP analysis, software flat-file generation, JSON file generation at digss level, and FV on all digital modules up to PD.
- Projects: Magnus 2.0, RIOT,

Design and Implementation of IOTFE

- Design and Implementation of the complete IOTFE module in RIOT project.
- Worked extensively on implementation of complex digital Top module and FV on all modules.
- Project: RIOT

Clock Domain Crossing Analysis:

- Worked on Clock Domain Crossing (CDC) of complete Digital Subsystem, creating constraints and waivers, reporting violations and providing solutions.
- Project: Cheops (Chiptop)

Jul 2013 – Dec 2016

SoCtronics Technologies, India | Engineer - Front End Design/Verification/Scripting

Responsible for the Front End Design, Verification and Scripting for various projects during the long tenure, in the capacity of Engineer I and Engineer II.

Verification of Thermal Sensor, Process Monitor:

- The thermal sensor is used to find the characteristics of the transistor, and a process monitor is used to find the delay of gates used in the ring oscillators. Entire designing was done as part of the Test Chip project which evaluated standard gates functionality in different nanometer technologies.
- Verified different digital modules in Thermal Sensor and integrated them to form Digital IP.
- Verified Process Monitor Verilog model containing 36 Ring Oscillators. Process Monitor finds the clock period for each clock produced by each ring oscillator.

Programming Languages:

C, C++

Protocols:

PIB Bus | RF Bus | AMBA (AXI, AHB) | I2S | SATA

Methodology:

UVM

EDUCATION QUALIFICATION:

- Master of Science in VLSI | VEDAIIT, Hyderabad India | 2013
- Bachelor of Technology in Electronics and Communication Engineering | JNTU, Hyderabad India | 2010
- Intermediate in MPC | AP Board of Intermediate Education

PROJECTS & ACHIEVEMENTS

Jun 2012 – Jun 2013

Design of SATA Controller | Master's Project

Under the supervision of **Principle Engineer from Invecas company**, designed the SATA Controller Transport Layer and Link Layer.

- Wrote the asynchronous FIFO RTL code for data storage and transmission.
- Designed FIS encoding and decoding in the transport layer.
- Designed CRC and SCRAMBLING in Link Layer
- Designed primitive encoding, decoding and link layer state machine

Achievements

- Received **Qualstar in Qualcomm 2018.**
- Chess champion of the year 2015 in the Soctronics, Makuta and Invecas companies competition.
- Chess Champion of SVIT College in Btech.
- Represented College in University level chess championship.
- Intercollege Cricket tournament winner team member during MS.
- Represented the interschool Chess Championship.

Design Automation of Memory Wrapper For 14nm memories and DAC Design:

- Wrote PERL script for the entire flow to automate the creation of memory of required size.
- Held responsible for the usage of the tool for creation of basic memory at required corners.
- Analyzed violations for created memory and communicated with the corresponding designers.
- Designed and Interconnected all these individual modules to form a Digital part of the DAC block. Here, the digital to analog converter module consisted of I2S interface, Interpolator, Delta-sigma modulator and DEM block.

Design Automation of Standard Cells:

- Designed the automation of standard cells creation for different technologies using perl scripting.
- Designed different Verilog templates for power and non-power standard cells.
- Scripted the heart block of the whole project which generated 168 kinds of different cells depending on the name of the cell.
- Customized the inputs, outputs and inputs names for each cell.

Verification of AHB2AXI Bridge:

- Led the team of 5 for the verification of AHB2AXI bridge for communication between AHB devices and AXI devices.
- Implemented and verified modules for AHB master interconnect, AXI slave interconnect and Protocol conversion blocks.